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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/800,013	03/15/2004	Hiroshi Tobisaka	FEC 121	6811

23995 7590 01/03/2007
RABIN & Berdo, PC
1101 14TH STREET, NW
SUITE 500
WASHINGTON, DC 20005

EXAMINER

LEJA, RONALD W

ART UNIT	PAPER NUMBER
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2836

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/03/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/800,013

Applicant(s)

TOBISAKA ET AL.

Examiner

Ronald W. Leja

Art Unit

2836

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 June 2005.
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1-7 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☒ The drawing(s) filed on 26 July 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 7/26/2004.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

The Abstract of the Disclosure is objected to because there appears to be a typographical error in the first line thereof. Correction is required. See MPEP § 608.01(b).

Figure 3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim 6 is objected to because of the following informalities: There is a lack of antecedent basis for "said diode". Appropriate correction is required.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the

examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kouno et al. (6,365,932).

Kouno et al. disclose a semiconductor device wherein a surge absorption element (D1) is in parallel with a transistor (Q1) (see Fig. 5) for bypassing the transistor during a surge condition. The surge absorption element is disclosed as having less sheet resistivity than the prior art and is designed to have high breakdown voltage and low turn-on resistance. In the "Brief Summary" it is disclosed that the design can be a lateral MOSFET transistor and parallel bypass diode (for Claim 6). The "Background" recites that use of zener diode for the surge absorption element is known (for Claim 6). In the "Brief Summary", the Reference discloses that the breakdown of the MOSFET is about 120 volts and the breakdown for the diode is about 70 volts (for Claims 2-4). Kouno et al. do not appear to specifically recite that resistance during breakdown of the absorber (D1) is smaller than its resistance during breakdown operation of the transistor or that secondary breakdown current of the absorber element is larger than secondary breakdown current of the transistor. However from the various characteristics pointed out above, it is the opinion of the Examiner that it would have been obvious to have the resistance of the absorption element smaller while it is in breakdown than when the transistor is breakdown, since one would not want the surge protection (surge absorption) affecting normal operations of the transistor, and hence, one would want current flow through the absorption element only when there is a surge and not otherwise. This then leads to the fact, that it would have been obvious to have the secondary breakdown current


larger in the absorption element larger than that of the transistor (for Claim 1) and larger than the surge current (for Claim 5), as the absorption element is intended to protect the transistor, and therefore, one would not want it to enter into thermal runaway sooner; this would effectively diminish the level of protection being offered to the transistor and one would want this level to be higher than any anticipated surge current so the intended protection is afforded. As far as Claim 7, Figure 5 illustrates the parallel transistor and surge absorption element within an IC; one external terminal is shown. However, it would have been obvious to protect any transistor with a parallel absorption element, as fairly taught, and thus, would encompass other designs, for example, one having a transistor coupled to both an Input and an Output terminal. This would lead to increased sales and reliable Ics.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ronald W. Leja whose telephone number is (571)272-2053. The examiner can normally be reached on Monday thru Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571)272-2800. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.


Ronald W. Leja
Primary Examiner
Art Unit 2836

rwl
December 23, 2006

12/23/06